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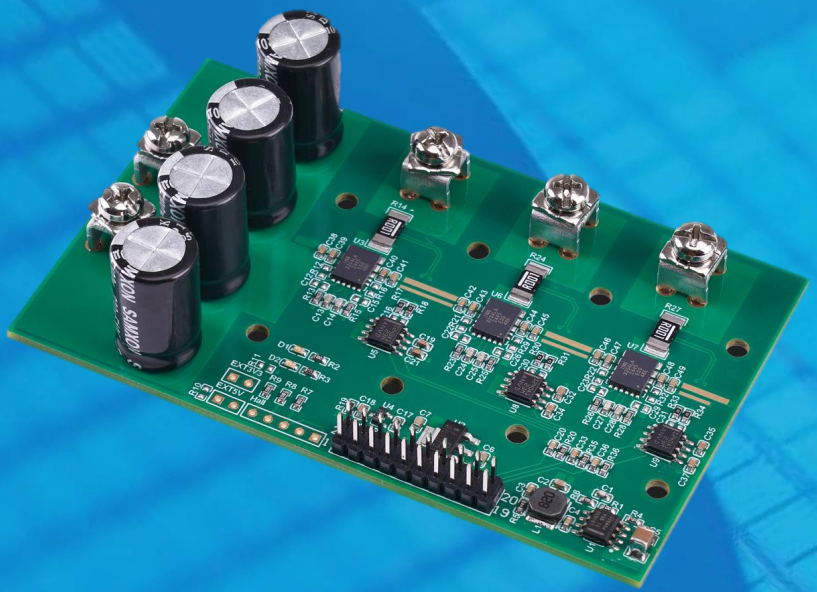
INNDDA500A2

Demo Manual

500W 48V Motor Drive

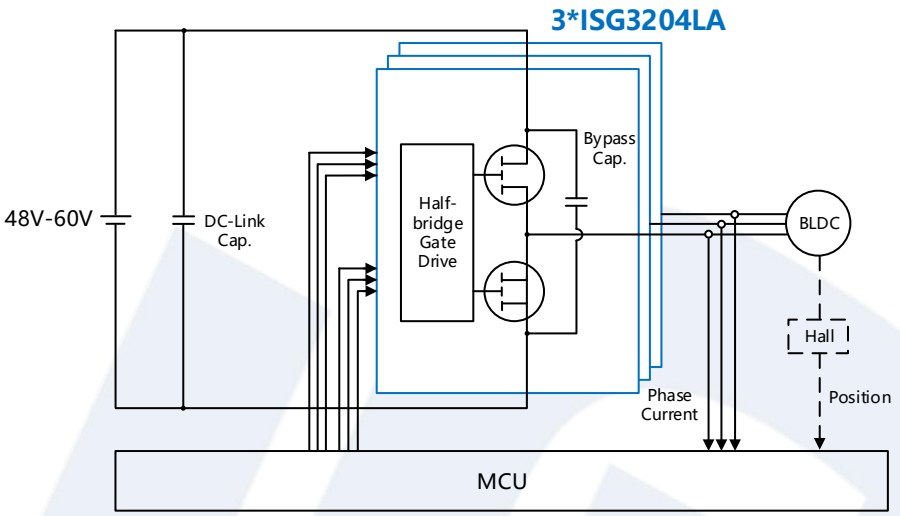
Featuring ISG3204LA



500W 48V Motor Drive

Three-Phase Motor Drive

Input voltage 48Vdc, continuous output current 35A.



Highlighted Products

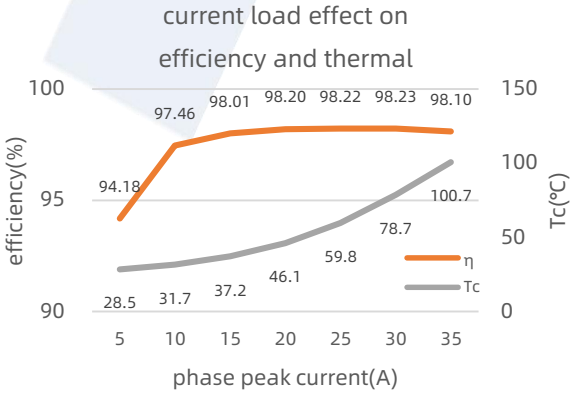
- ISG3204LA

Target Applications

- Robotics
- Drones
- eMobility

Photo

Test Result



List of Content

1. Overview

1.1. Description

The INNDDA500A2 comprises a three-phase motor drive. The measured continuous output current is 35A with extremely low total harmonics distortion (THD) around 0.6%. Efficiency is 97.54% even at 100kHz. The demo board size is 95mm×70mm×45mm.

1.2. Features

- Main features and Advantages
  - > Small Size: demo board is 95mm×70mm×45mm
  - > High efficiency: inverter efficiency is 97.54% even at 100kHz
  - > Low THD: extremely low THD around 0.6%

1.3. Applications

- Robotics
- Drones
- eMobility

2. Parameters

Table 1 Electrical characteristics (Ta=25℃)

Symbol	Parameter	Condition	Min	Nom	Max	Unit
System Specifications						
V_{in}	Input voltage		24	48	60	V_{dc}
F_s	Switching frequency		0	20	100	kHz
T_d	Dead time		20	50		ns
I_{OUT}	Output current			25	35	A
P_{OUT}	Output power			500	1000	W
Demo Performance						
THD	Total harmonics distortion	Measured @V_{in}=48V_{dc}, I_{out}=24A, F_s=100kHz, T_d=100ns		0.6		%
Eff	efficiency	Measured @V_{in}=48V_{dc}, I_{out} =25A, F_s=20kHz, T_d=20ns		98.2		%

3. Demo Solutions

3.1. Topology

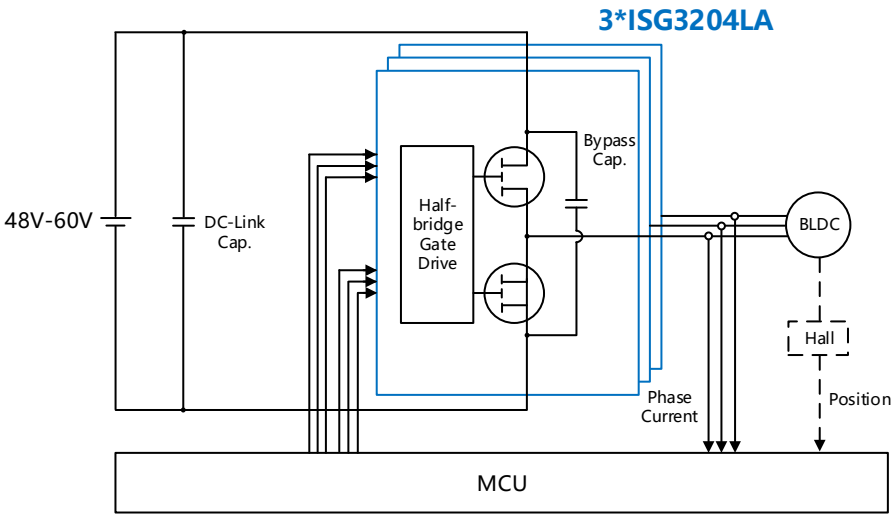


Figure 1 500W 48V three-phase motor drive topology

The INNDDA500A2 comprises a three-phase half bridge.

3.2. Value of InnoGaN

InnoGaN offer improved performance over silicon MOSFET due to several key characteristics:

- Gate Charge Q_g

Comparing InnoGaN to silicon MOSFET with the same R_{on}, GaN have about seven times lower Q_g than silicon MOSFET. Lower Q_g means faster turn on and turn off speed, resulting in lower switching loss and driver loss. At the same time, fast turn on and off speed can help to reduce dead time which will lead to lower THD, reducing torque ripple and noise of motor.

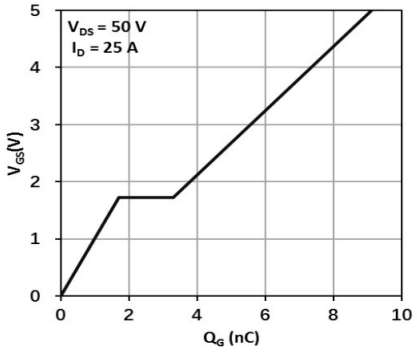
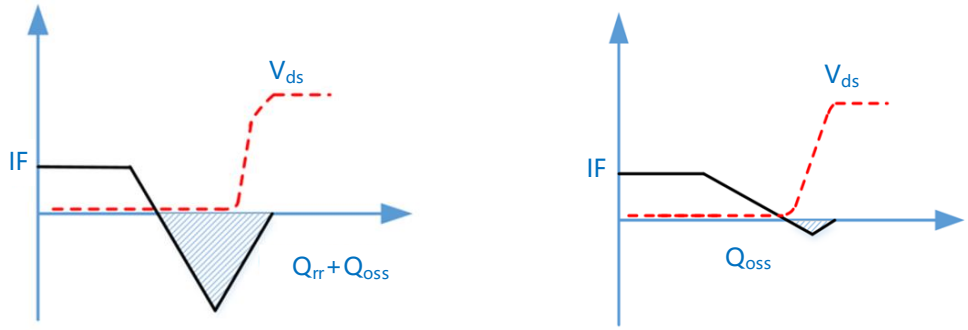


Figure 2 Typical gate charge

■ Reverse Recovery Charge Q_{rr}

Si MOSFET have intrinsic body diode structures with a large reverse recovery charge which will lead to additional loss. InnoGaN have no Q_{rr} because there are no minority carriers in the channel to recover, which makes it an ideal fit for motor drives.



(a)Si MOSFET (b) InnoGaN

Figure 3 Turn off transition

3.3. Highlighted Products

3.3.1. InnoGaN Device ISG3204LA

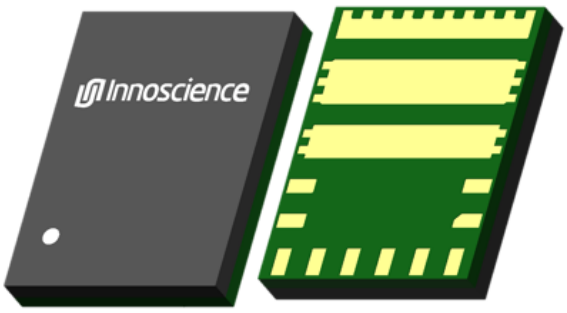


Figure 4 InnoGaN device ISG3204LA

InnoGaN Device ISG3204LA is in LGA(Land Grid Array) package, comprising a half bridge driver and two GaN devices with maximum conduction resistance of 3.2mΩ. The product meets the requirements of more compact, lower loss, higher power design applications.

4. Hardware Implementation

4.1. Hardware Introduction

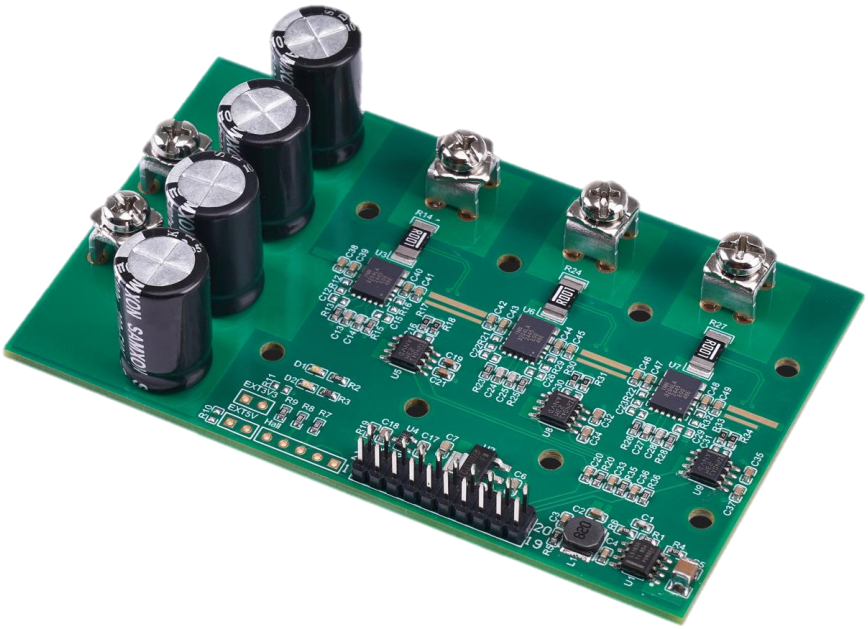


Figure 5 500W 48V motor drive

The 500W 48V motor drive demo board is shown as Figure 5. The reference design consists of following sub-assemblies:

1) **Three-phase Half Bridge:** This board consists of 3 ISG3204LA which comprises half bridge GaN HEMTs and drivers.

2) **Current Sensing:** This board consists of Three-phase current sensing resistors and conditioning circuit.

3) **Auxiliary Power Supply:** This board consists of Auxiliary power supply which is used to provide power supply for control circuit and drivers.

4.2. Design Considerations

4.2.1. InnoGaN Layout Recommendation

The GaN HEMTs feature very small input capacitance: i.e. a very small gate capacitance and miller capacitance. Therefore, The GaN HEMTs can operate with very-fast-speed switching: i.e. high dv/dt and high di/dt. In order to avoid the voltage and current spike caused by high dv/dt and high di/dt, the parasitic of the gate driving loop and power loop must be reduced by proper

layout technique. ISG3204LA employs an excellent layout on internal substrate to reduce the gate driving loop and power loop: (1) the driver has been placed very close to the GaN HEMTs to minimize the loops of parasitic inductance and reduce the noise on the gate loop. (2) the bootstrap capacitor is integrated in the module and the distance between BST and VCC to the driver has been minimized which avoids the possible high peak current during recharging time. (3) the distance between high-side GaN FET and low-side GaN FET has been minimized to avoid excessive negative voltage to the driver caused by the parasitic inductance between high-side GaN HEMT and low-side GaN HEMT.

Although the optimized pinout of ISG3204LA simplifies the power stage layout significantly, to fully utilize the benefit of ISG3204LA, A good power board layout is still necessary. The layout guidelines are as follows:

1. The optional resistor between HGP(LGP) pin and HG(LG) pin to adjust the turn-on speed of the GaN HEMT should be placed close to ISG3204LA.

2. The optional VCC decoupling capacitor should be placed close to ISG3204LA.

3. The power input decoupling caps should be placed close to Vin bar and PGND bar. One 4-layer layout example is shown as Figure 6. 2-layer board design is also possible thanks to the optimized ISG3204LA pinout.

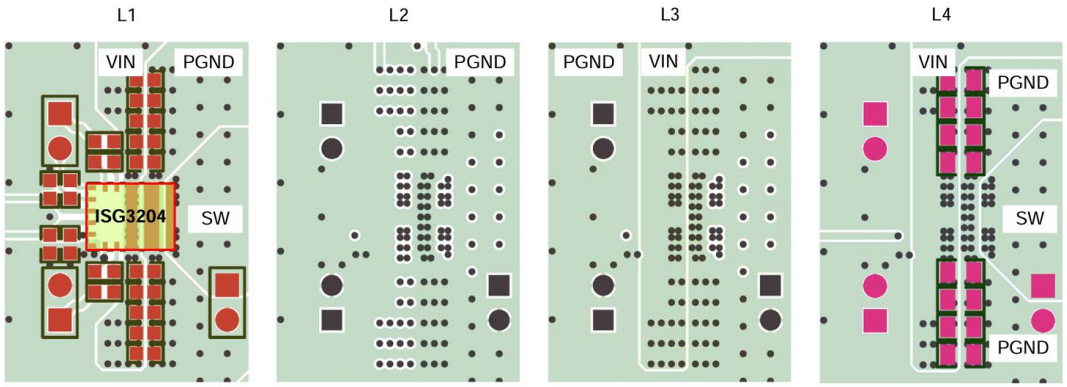


Figure 6 4-Layer Layout Example

4.3. Test Results

4.3.1. THD

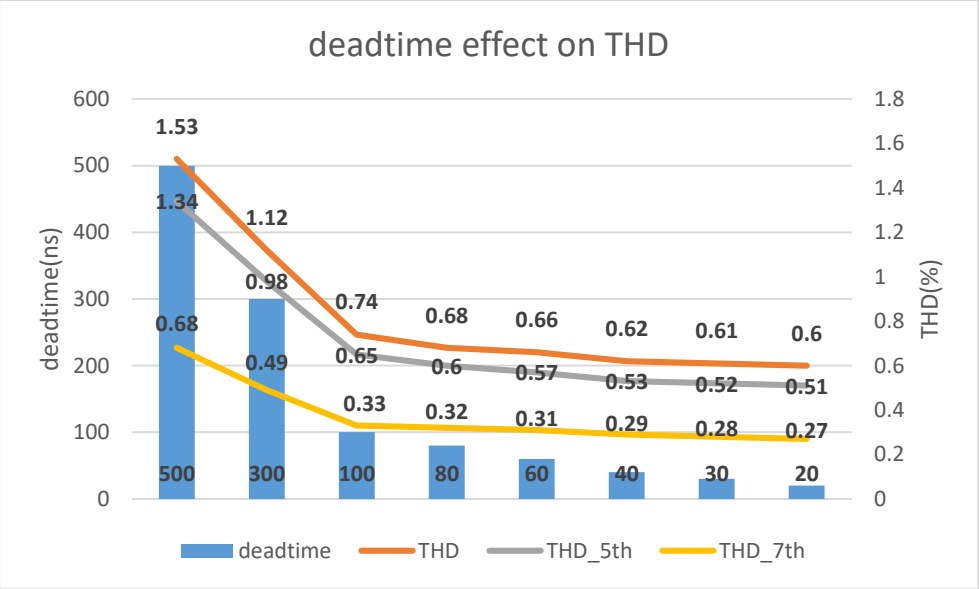


Figure 7 Curves of motor drive

dead time of GaN-based inverters can be reduced from 1μs to 20ns, resulting in 5-th harmonics reduced from 1.34% to 0.51% and 7-th harmonics reduced from 0.68% to 0.27%. This helps motor to show perfect THD even at very low speed.

4.3.2. Thermal Test

INNDDA500A2's thermal performance is tested under natural convection with heatsink. INNDDA500A2 can reach maximum efficiency of 98.23%, phase peak current can reach 35A with total 1000W output when Tc≈100℃ as shown in figure 8.

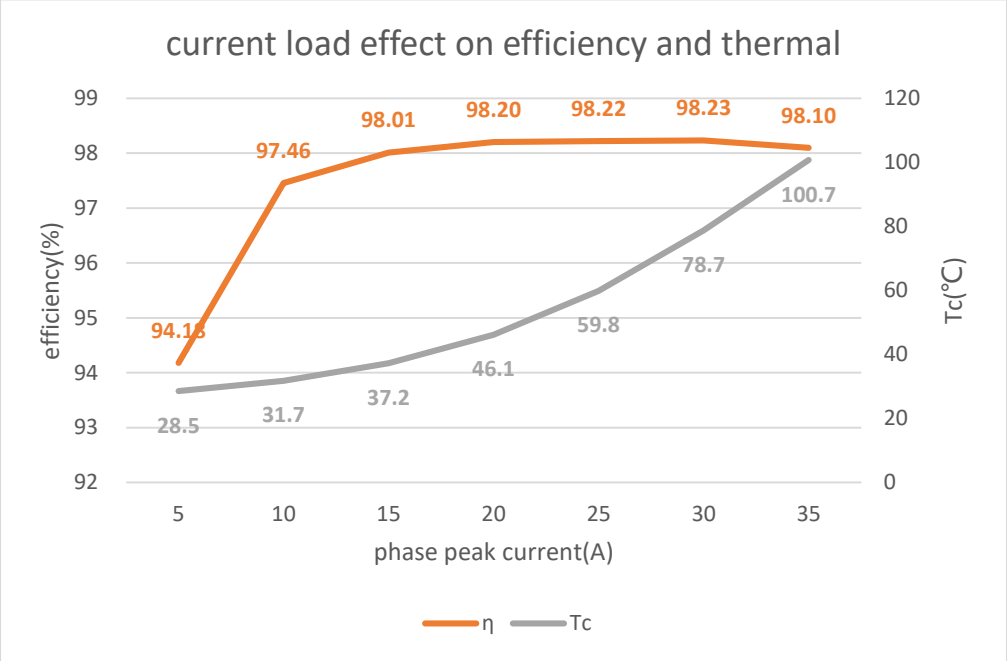
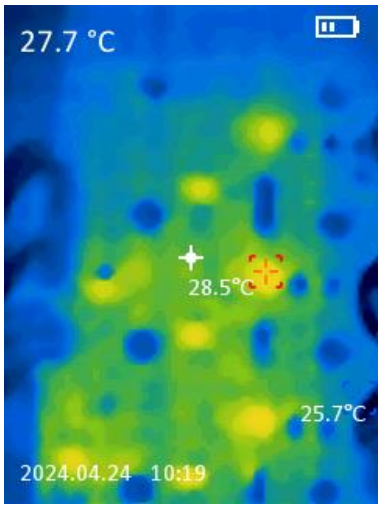
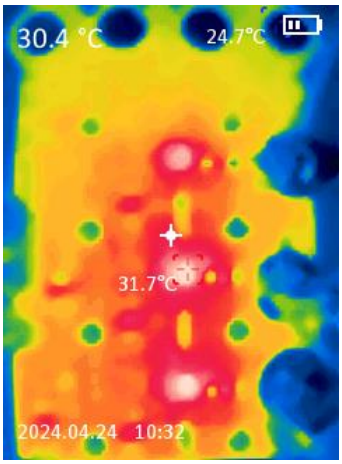
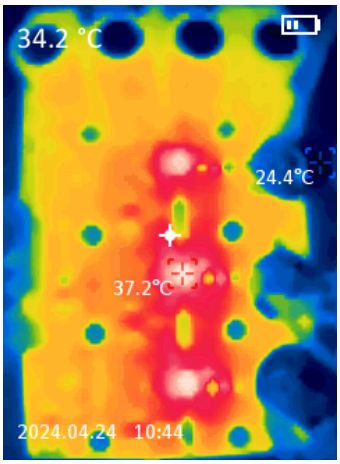
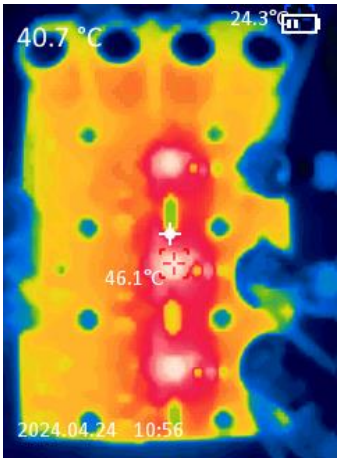


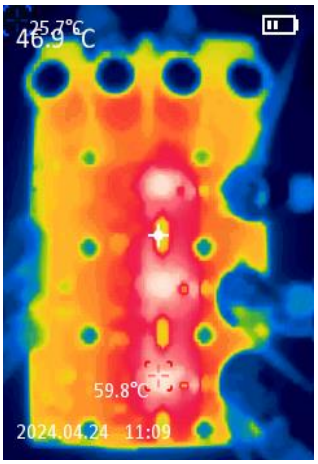
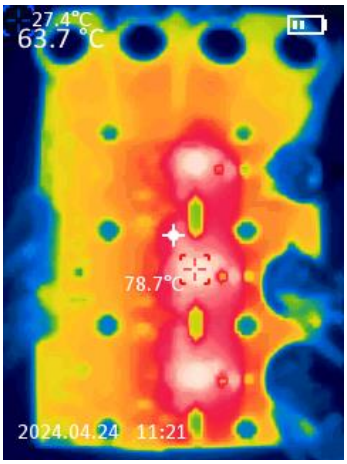
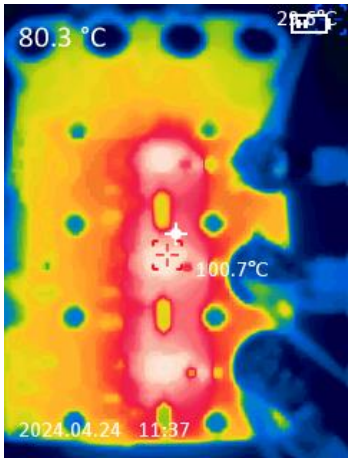
Figure 8 Curves of motor drive

Detailed thermal result is illustrated in table 2.

Table 2 Inverter test conditions

	**Test condition** V_{in}=48V I_p=5A F_s=20kHz T_d=20ns **Test result** T_c=28.5℃

	**Test condition** V_{in}=48V I_p=10A F_s=20kHz T_d=20ns **Test result** T_c=31.7℃
	**Test condition** V_{in}=48V I_p=15A F_s=20kHz T_d=20ns **Test result** T_c=37.2℃
	**Test condition** V_{in}=48V I_p=20A F_s=20kHz T_d=20ns **Test result** T_c=46.1℃

	**Test condition** V_{in}=48V I_p=25A F_s=20kHz T_d=20ns **Test result** T_c=59.8℃
	**Test condition** V_{in}=48V I_p=30A F_s=20kHz T_d=20ns **Test result** T_c=78.7℃
	**Test condition** V_{in}=48V I_p=35A F_s=20kHz T_d=20ns **Test result** T_c=100.7℃

GaN HEMT can operate in high switching frequency with little thermal penalty because of low switching loss, switching frequency of INNDDA500A2 can increase from 20kHz to 100kHz with only 25℃ rise in temperature as shown in figure 9.

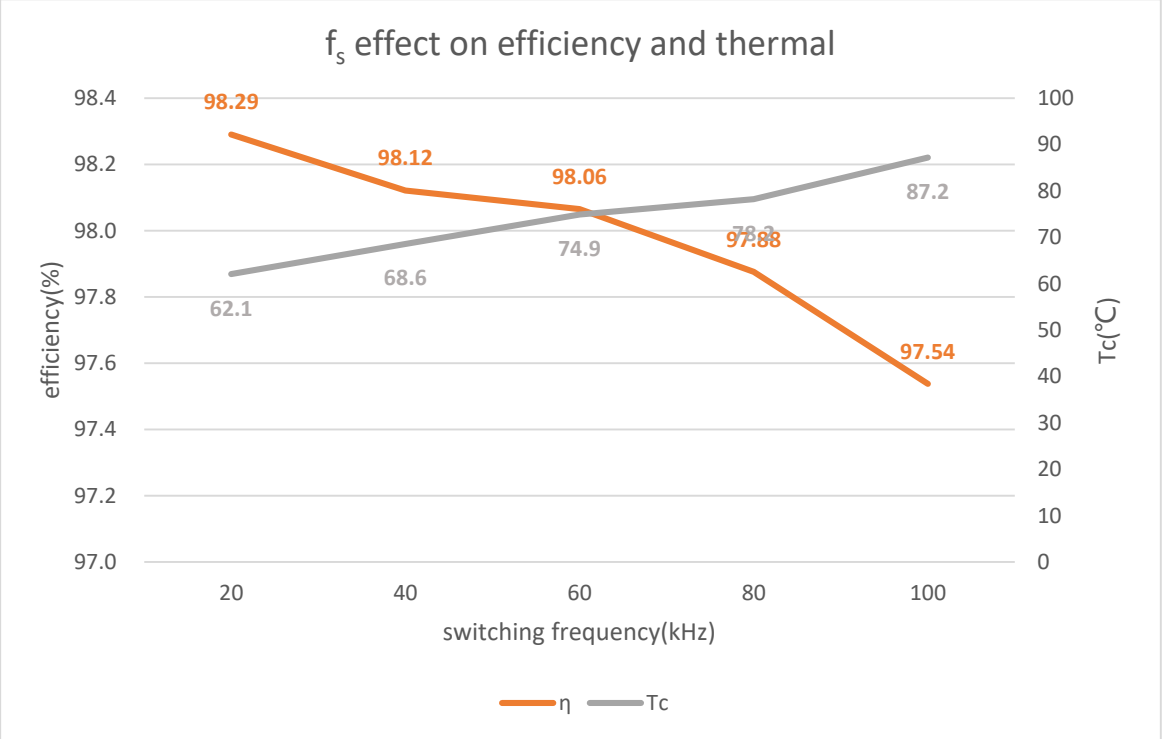


Figure 9 Effect on efficiency and thermal

Appendix

Appendix A. Testing guidance

1. Test condition

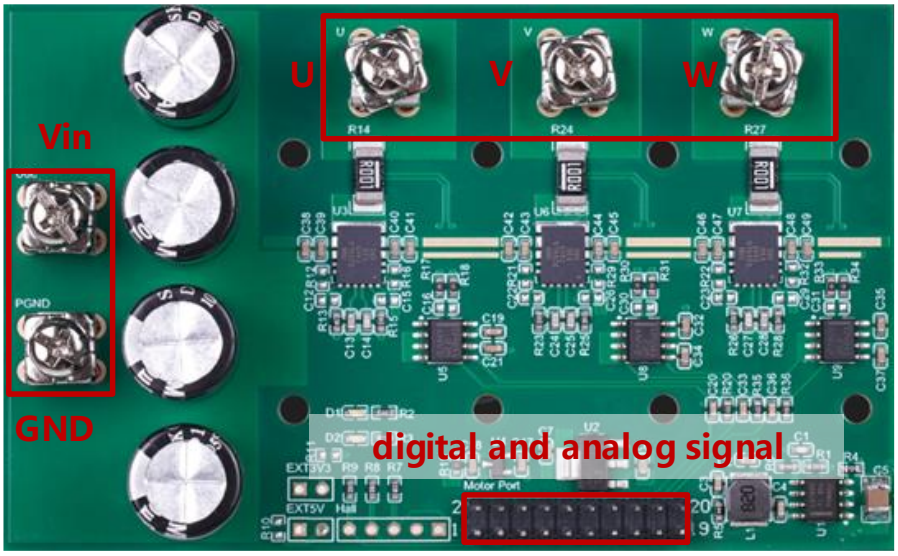
INNDDA500A2 is designed mainly for evaluation of InnoGaN performance on three-phase motor drive and provides reference solution for power stage. Demo board can be connected to control board to realize close loop control of motor.

Detailed test conditions are listed in appendix table 1.

Appendix Table 1 Inverter test condition

Symbol	Parameter	Value	Unit
V_{dc}	DC-bus voltage	48	V
P_{out}	Rated output power	500	W
$P_{out,pk}$	Peak output power	1000	W
f_0	Fundamental frequency	150	Hz
f_s	Switching frequency	20	kHz
T_d	Dead time	20	ns

2. Test point location and wiring diagram



Appendix Figure 1 Test point location and wiring diagram

Appendix Table 2 Description of digital and analog signal pin

Pin	2	4	6	8	10	12	14	16	18	20
Description	PWMHU	PWMLU	PWMHV	PWMLV	PWMHW	PWMLW	GND	GND	IV	GND
Pin	1	3	5	7	9	11	13	15	17	19
Description	ENC_H1	ENC_H2	ENC_H3	GND	GND	GND	GND	IU	IW	GND
PWMXX	PWM signal									
ENC_HX	level shift for encoder									
IX	current sample signal									

3. Power up and down sequence

1.Ensure all the power supplies are off.

2.Connect the DC voltage source to terminal Vin and common ground terminal GND.

3.Connect the Motor or RL load to UVW output terminal.

4.Connect the controller to demo board including PWM signals, analog signals and GND.

5.Turn on the controller and output the PWM signal with the required duty ratio and frequency, ensure PWM input of each ISG3204LA is same as controller output.

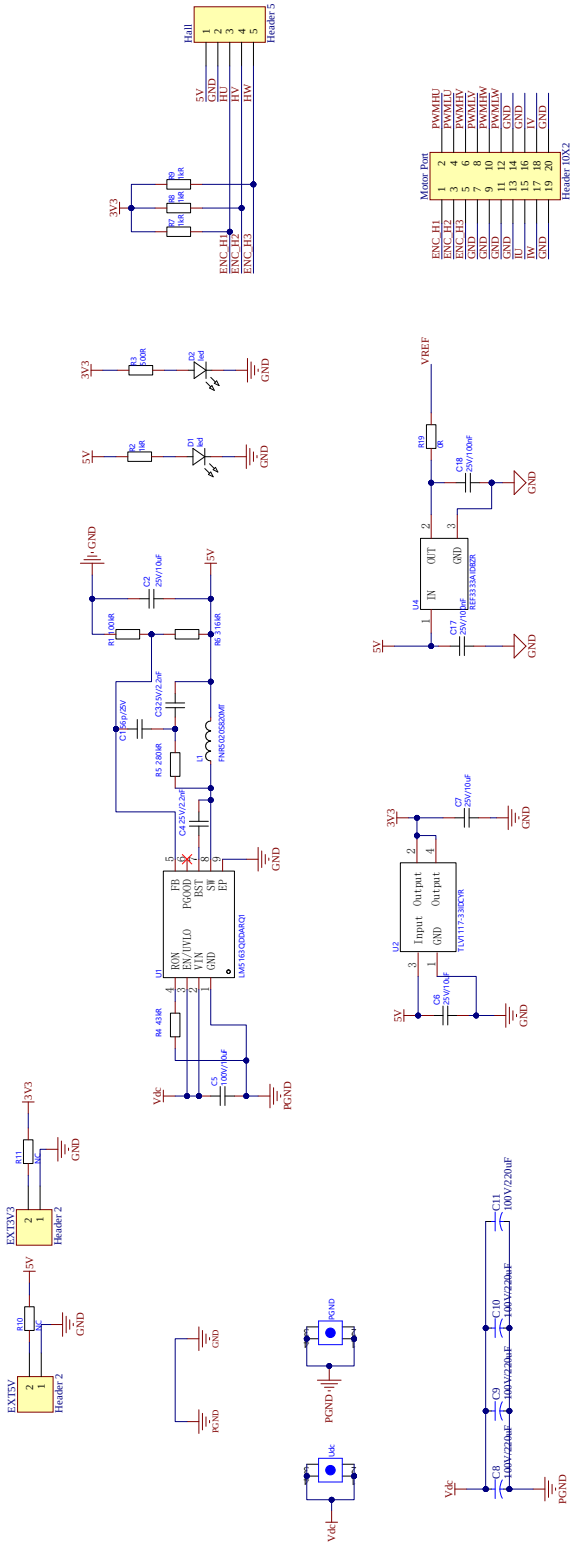
6.Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage).

7.Ensure three-phase SW waveforms are correct before controlling motor as wanted.

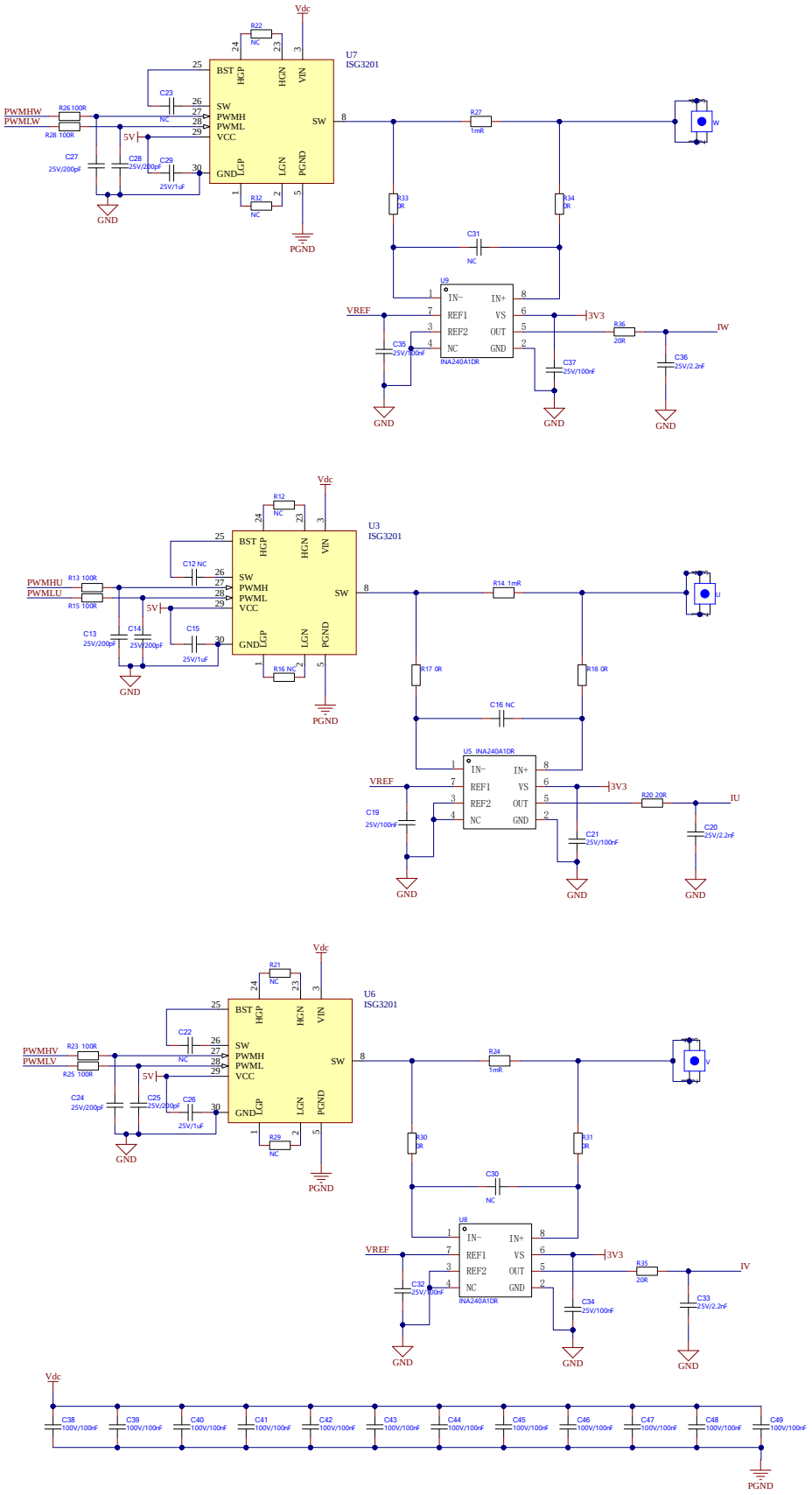
8.Turn off the DC voltage source if all measurement is done.

9.Turn off the controller.

Appendix B. Schematic

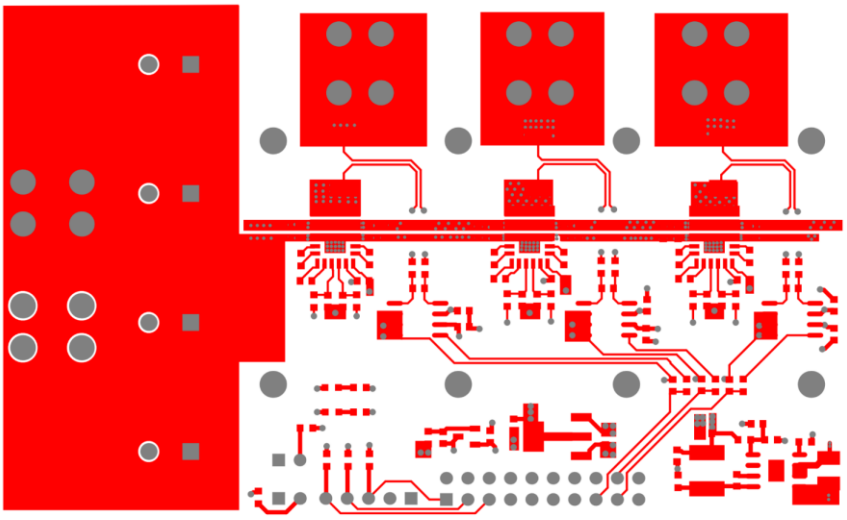


Appendix Figure 2 Schematic(1)

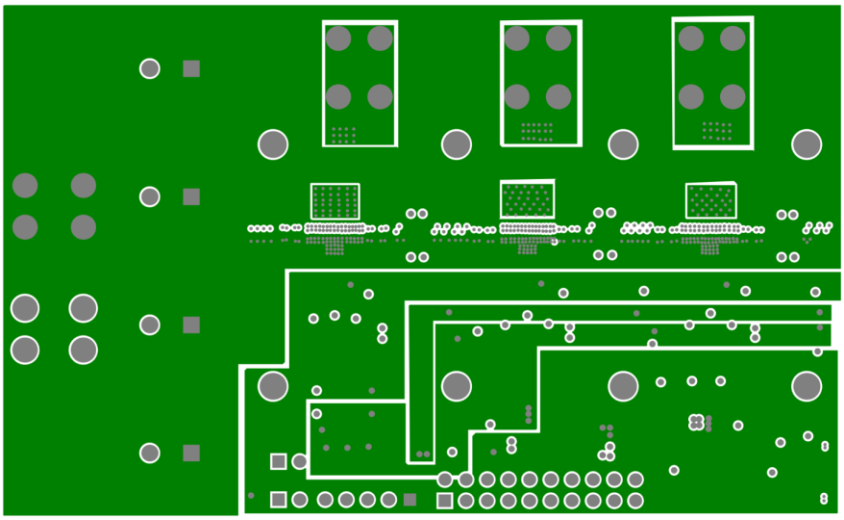


Appendix Figure 3 Schematic(2)

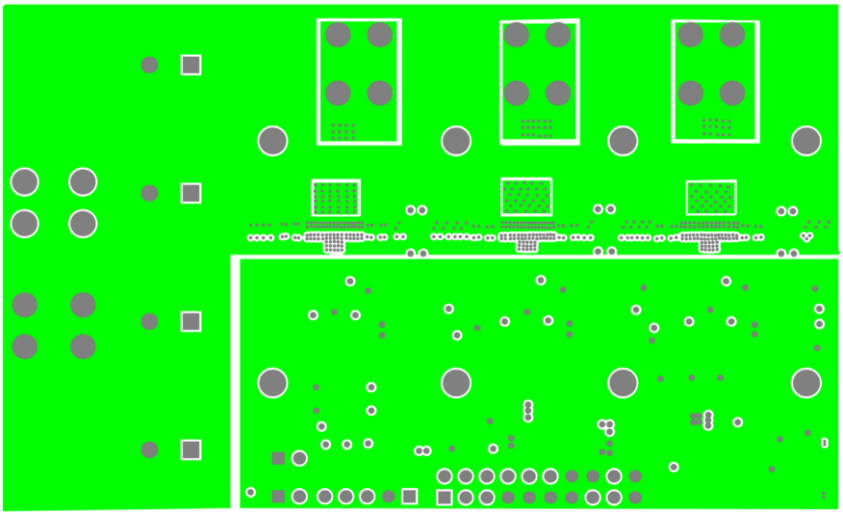
Appendix C. PCB Layout



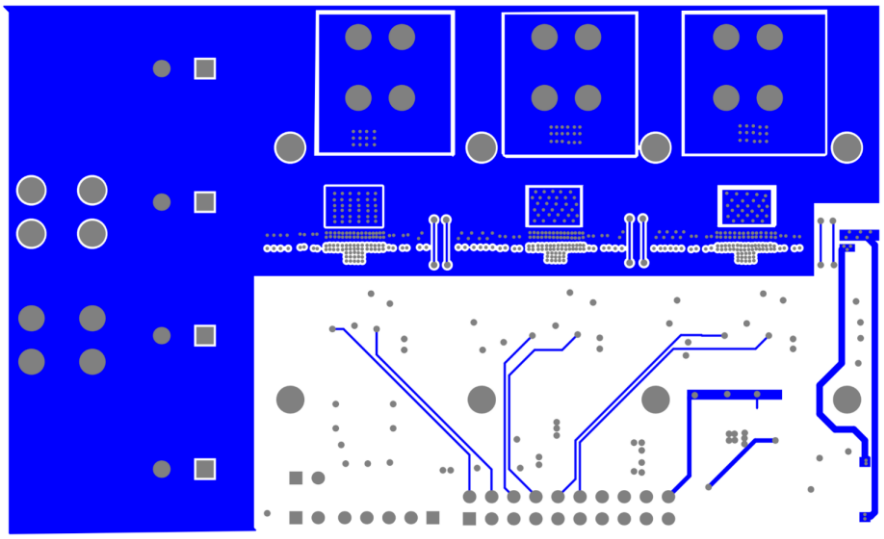
Appendix Figure 4 Top Overlayer



Appendix Figure 5 Mid1 Layer



Appendix Figure 6 Mid2 Layer



Appendix Figure 7 Bottom Layer

Appendix D. BOM

Part Number	Manufacture	Description	Dsignator	Footprint	Quantity
C0603X560K3HAC7867	KEMET	CAP, 56p/25V, ±10%, X8R	C1	C0603	1
GRM188R61E106KA73D	muRate	CAP, 10u/25V, ±5%, C0G	C2, C6, C7	C0603	3
CC0603KRX7R8BB222	YAGEO	CAP, 2.2n/25V, ±10%, X7R	C3, C4, C20, C33, C36	C0603	5
GRM32EC72A106KE05L	muRate	CAP,10u/100V, ±10%, X7S	C5	C1210	1
ERJ1KM221W20OT	AISHI	CAP,220u/100V E-cap	C8, C9, C10, C11	DIP_D12.5xL20	4
CC0603KRX7R8BB221	YAGEO	CAP, 220p/25V, ±10%, X7R	C13, C14, C24, C25, C27, C28	C0603	6
CC0603KRX5R8BB105	YAGEO	CAP,1u/25V, ±10%, X5R	C15, C26, C29	C0603	3
CC0603KRX7R8BB104	YAGEO	CAP,100n/25V, ±10%, X7R	C17, C18, C19, C21, C32, C34, C35, C37	C0603	8
CC0603KRX7R0BB104	YAGEO	CAP,100n/100V, ±10%, X7R	C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49	C0603	12
RC0603FR-07100KL	YAGEO	RES, 100kR, ±1%, 100mW	R1	R0603	1
RC0603FR-071KL	YAGEO	RES, 1kR, ±1%, 100mW	R2, R7, R8, R9	R0603	4
RT0603BRC07500RL	YAGEO	RES, 500R, ±1%, 100mW	R3	R0603	1
RT0603BRD0743KL	YAGEO	RES, 43kR, ±0.1%, 100mW	R4	R0603	1
RT0603BRD07280KL	YAGEO	RES, 280kR, ±0.1%, 100mW	R5	R0603	1
RC0603FR-07316KL	YAGEO	RES, 316kR, ±0.1%, 100mW	R6	R0603	1
RC0603FR-07100RL	YAGEO	RES, 100R, ±0.1%, 100mW	R13, R15, R23, R25, R26, R28	R0603	6
RC0603FR-070RL	YAGEO	RES, 0R, ±1%, 100mW	R17, R18, R19, R30, R31, R33, R34	R0603	7
RC0603FR-0720RL	YAGEO	RES, 20R, ±1%, 100mW	R20, R35, R36	R0603	3
HoJLR2512-3W-1mR	Milliohm	RES, 100R, ±1%, 3W	R14, R24, R27	R2512	3
NCD0603B1		LED	D1, D2	led0603	2
FNR5020S820MT	cjiang	Inductor,82μH/750mA	L1	SMD,5x5mm	1
Header 10X2		Header, 10-Pin, Dual row	Motor Port	HDR2X10	1
ISG3201	Innoscience	100V Half-Bridge Solid-GaN Integrating Gate Driver	U3, U6, U7	LGA_5_6	3
LM5163QDDARQ1	TI	Buck	U1	ESOP_8	1
TLV1117-33IDCYR	TI	LDO	U2	SOT_223	1
REF3333AIDBZR	TI	Voltage Reference	U4	SOT_23_3	1
INA240A1DR	TI	Current Sense Amplifier	U5, U8, U9	SOIC_8	3
Header 2		Header, 2-Pin	EXT3V3, EXT5V	Header 2	2
Header 5		Header, 5-Pin	Hall	Header 5	1
NC			C12, C16, C22, C23, C30, C31	C0603	6
NC			R10, R11, R12, R16, R21, R22, R29, R32	R0603	8

Revision History

Date	Versions	Description	Author
2023/08/21	1.0	First edition	SE team
2023/11/08	1.1	Uadate thermal test results	SE team
2025/01/13	2.0	Second edition, use phase current sensing, update efficiency test results	AE team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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